UNIVERSITY COLLEGE LONDON

University of London

EXAMINATION FOR INTERNAL STUDENTS

For The Following Qualification:-

B.Sc.

Physics 3C75: Principles and Practice of Electronics

COURSE CODE	:	**PHYS3C75**
UNIT VALUE	:	**0.50**
DATE	:	**25-MAY-06**
TIME	:	**10.00**
TIME ALLOWED	:	**2 Hours 30 Minutes**

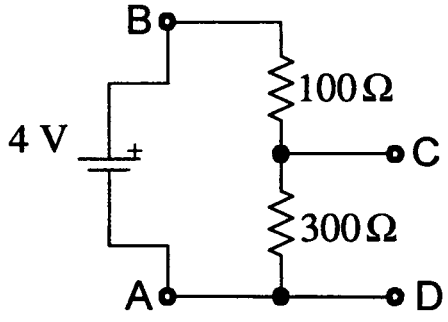
TURN OVER

Answer ALL SIX questions in Section A and TWO of the questions from Section B.

The numbers in square brackets in the right-hand margin indicate the provisional allocation of maximum marks per sub-section of a question.

Section A

1 (a) For the potential divider shown in the circuit below, identify the *input terminals* and the *output terminals*. [1]



(b) Find the potential appearing between terminals C-D when no load is connected. [2]

(c) Find the current that would flow through a short circuit link connected between C and D. [1]

(d) Draw a (general) Norton equivalent circuit, labelling the components appropriately. [1]

(e) Using the results found in (b) and (c) or otherwise, find the Norton equivalent *current source* and the Norton equivalent *internal resistance* for the given potential divider. [2]

2. (a) Draw the circuit symbols for the following logic gates, label all of the terminals, and give the Boolean equation for each:

(i) 2-input AND,
(ii) 2-input OR,
(iii) 2-input NOR,
(iv) 2-input NAND,
(v) NOT. [4]

(b) Write down any one of the de Morgan theorems for two variables and draw the circuits that represent each side of the equation in terms of logic gates. [3]

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3. Draw the circuit of an *SR latch* in terms of two 2-input NAND gates and two NOT gates. Label the inputs and outputs correctly using the conventional symbols S, R, Q, $\overline{Q}$. [2]

Use truth tables to clearly demonstrate that the state Q=0 is consistent with S, R=0, 0 and with S, R=0, 1 and that the state Q=1 is consistent with S, R=0, 0 and with S, R=1, 0. Determine the value of $\overline{Q}$ in each of the four cases. [3]

Use the above results to briefly explain how the SR latch is used. [2]

4. Briefly describe the characteristics and functions of the *semiconductor junction diode.* [2]

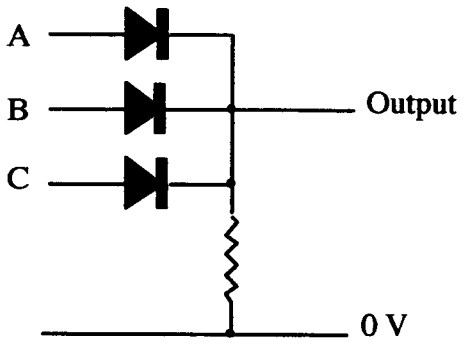
For the circuit below, determine the output voltage in each of the following cases (you may assume that a forward biased diode has a voltage drop of 0.6 V):

(i) $V_A = V_B = V_C = +5\,\text{V}$

(ii) $V_A = V_B = 0\text{V};\ V_C = +5\,\text{V}$

(iii) $V_A = 0\text{V};\ V_B = +0.1\text{V};\ V_C = +0.2\,\text{V}$

(iv) $V_A = V_B = -2\text{V};\ V_C = +1\,\text{V}$. [4]



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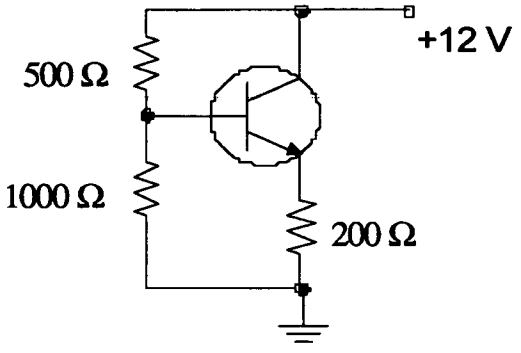
5. (a) For the circuit below, label the base, collector and emitter of the transistor as *b, c, e* respectively. [1]



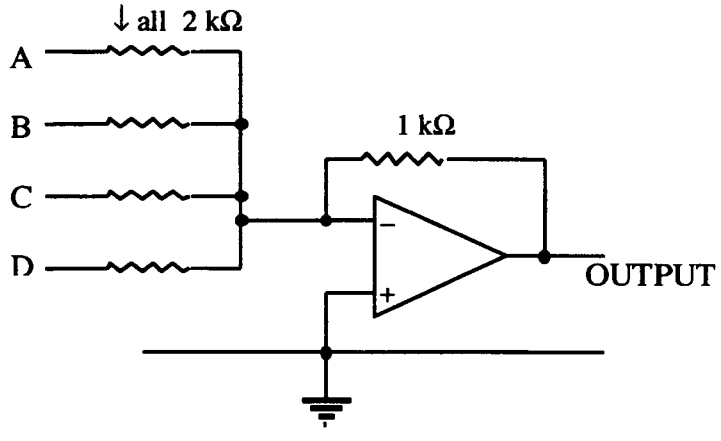
(b) Estimate the base voltage, stating any assumptions or approximations that you make. [2]

(c) Estimate the emitter voltage, stating any assumptions or approximations that you make. [1]

(d) Find the emitter current. [1]

(e) If the current gain β of the transistor is 150, determine whether the assumptions or approximations that you made in (b) are valid. [2]

6. What is the purpose of the operational amplifier circuit shown below? Indicate the position on the diagram of the *virtual earth.* [2]



Derive the equation relating the output voltage to the four input voltages *A, B, C, D.* [4]

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Section B

7. Explain the meaning of the term *change function* for a sequential digital circuit and show that the Boolean expression for the change function of a J K flip-flop is $J\overline{Q} + KQ$. [5]

Describe the D flip-flop and the T flip-flop and show how each may be implemented using a J K flip-flop. [3]

Determine how many flip-flops are required for a synchronous counter that will count up from 0 to 5 and then reset to 0, i.e. count through the sequence 0, 1, 2, 3, 4, 5, 0, 1... and write out the truth table for the flip-flop change functions. You may assume that the counter is always correctly initialised to the state "0" before counting begins. [7]

Specify an appropriate type of flip-flop to implement the counter. Determine the minimal logic for each change function. [10]

Establish the input logic for each flip-flop and draw the final circuit diagram of the counter. [5]

8. Outline the behaviour of the *analogue comparator* and explain its importance for analogue-to-digital conversion circuits. [5]

Describe in detail the mode of operation of a three bit successive approximation ADC, using schematic diagrams and timing diagrams wherever appropriate. [You do not need to describe the internal logic of the sequencing circuit.] [20]

Briefly describe the mode of operation of the flash ADC and state for which kinds of application it might be preferred over the successive approximation ADC. What desirable characteristic(s) does the successive approximation ADC have compared to the flash ADC of the same number of bits? [5]

9. Write down the mathematical relationship that describes the characteristics of an "ideal" operational amplifier and explain the terms used with reference to the standard circuit symbol. [5]

State what is meant by a *virtual earth* in an operational amplifier circuit and derive the two design equations for a virtual earth circuit. [7]

Draw the operational amplifier circuits that perform the following functions. Include appropriate values for all of the passive components used.

(i) Inverting voltage amplifier with a gain of 500. [3]
(ii) Non-inverting amplifier with voltage gain of 5. [4]
(iii) Inverting integrator with a time constant of 12 ms. [5]
(iv) Difference voltage amplifier with a gain of 20. [6]

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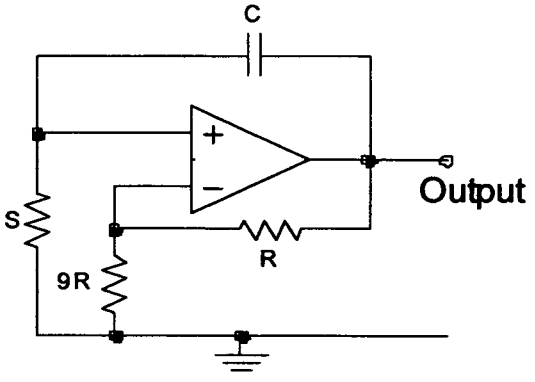
10. Derive the equation relating the input signal voltage to the output signal voltage for an amplifier circuit using voltage-derived series-applied negative feedback. [10]

Explain under what conditions such a circuit becomes a positive feedback circuit and state, without giving quantitative details, what the consequences of this would be. [5]

The circuit given below is a *multivibrator*. Not shown are the power supply connections to the op amp which you should take to be +10 V and −10 V. Describe in detail how the multivibrator operates, stating the relevant voltage levels, and illustrate this using a time-voltage diagram. [10]



Explain without giving detailed formulae how the period of oscillation would depend on the values of the components in the circuit. [5]

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